

REMARKS

Withdrawal of the outstanding rejections and early allowance of the above-identified application in consideration of this submission is respectfully requested.

With this filing claims 16-38 are pending of which claims 16 and 17 are currently amended and claims 29-38 are newly presented. (Claims 1-15 were earlier canceled.) Base claim 16 was amended to further define the invention including in a manner which clearly highlights the patentable differences of applicants invention over that taught by the art as cited in the outstanding Office Action. In base claim 16, a number of editorially formatting revisions were also implemented therein which will become clearly understood with the further discussion, which follows. In dependent claim 17, the revisions therein are of an obvious grammatical nature. The new claims were presented in consideration of more fully covering the various originally disclosed inventive aspects including various permutations directed thereto and related to that covered by the set forth "memory card" according to claims 16-28.

The invention according to claims 16+ and, also, according to new claims 29+ and 38, are directed to a memory card such as that shown in Figs. 7-8 of the drawings, in which a control chip 1B is stacked on one memory chip or on a stacked plural memory chips such as flash memory chips, which are, in turn, mounted on a substrate (e.g., base substrate 2), although not limited thereto. As can be seen from Figs. 7-8, as one example thereof, the memory card MC contains a memory chip or a stacked arrangement of memory chips 1A mounted on the main surface of the substrate and contains, also, another semiconductor chip such as control chip 1B which is stacked over the main surface of the memory chip 1A, consistent with that called for in each of the independent claims 16, 29 and 38. Adoption of such a chip stacking scheme on a substrate such as base substrate 2 makes it possible to

decrease the dimensions of the base substrate which, in turn, leads to a reduced size and weight of the memory card (see paragraphs [0056] - [0057] on page 13 of the Specification. As a counter measure to the additional thickness resulting from the stacking of the "second semiconductor chip" such as the control chip 1B on the "first semiconductor chip" or the memory chip 1A, an increase in the thickness of the resin sealant can be suppressed by polishing the respective rear surfaces of the stacked chips to effectively reduce the thicknesses thereof (see paragraph [0058] of the Specification and also claims 19, 21 and 25).

A further aspect of the currently amended claims differentiates the set of wires for electrically connecting the bonding pads associated with the "first semiconductor chip" (e.g., memory chip 1A) to a corresponding set of electrodes on the main surface of the substrate from the set of wires for electrically connecting the bonding pads of the "second semiconductor chip" to a set of different electrodes on the main surface of the substrate. As can be seen from Figs. 7 and 8 of the drawings, the set of wires 6 which electrically connect the bonding pads of the memory chips 1A (or "first semiconductor chip") to the corresponding set of electrodes (or "plurality of first electrodes") on the main surface of the substrate 2 relate to the set forth "first wires," and wires 6 which electrically connect bonding pads of the control chip 1B (or "second semiconductor chip") with corresponding ones of electrodes 5 (or a "plurality of second electrodes") relate to the set forth "second wires," according to independent claims 16, 29 and 38.

With regard to independent claim 16, it is further characterized by a bonding wiring scheme in which the first wires are crossing over one side of the first semiconductor chip and the second wires are crossing over another side of the semiconductor chip, in the plan view thereof. As to the former, this can be seen by wires 6 which are crossing over the left side (i.e., left side peripheral edge) of the

memory chip 1A. Regarding the latter, wires 6 in Fig. 8 which are positioned along the right side and/or upper/lower sides of the memory chip 1A, of the plan view illustration Fig. 8, are relating thereto. Due to such a schemed construction, the loop height of the "second wire," can thereby be reduced, which is clearly desirable. If, however, the "second wires," associated with the external connections of the control chip or "second semiconductor chip", are formed on the same side, crossing over the same peripheral edge as that of the "first wires," the loop height of the "second wires" would necessarily be increased in order to prevent contact between ones of the "first wires" with ones of the "second wires." Such would retard attempts at further reduction of size/thickness of the memory card. The just discussed featured aspects directed to the last two "wherein" clauses of independent claim 16 are now also contained in newly presented independent claim 38.

According to new independent claim 29, the set forth featured aspects of independent claim 16 are specifically specified therein except for the above-discussed "wherein" clauses in independent claim 16. However, claim 29 does require that the "first electrodes" and the "second electrodes", which are formed on the main surface of the substrate, are positioned along respectively different sides of the mounted first semiconductor chip. With regard to the set forth "first electrodes ... along one side of the mounted first semiconductor chip", the arrayed external terminals 5 along the left side of the memory chip 1A in the plan view showing in Fig. 8 is an example thereof. Regarding the set forth "second electrodes ... along another side of the mounted first semiconductor chip", the set of external electrodes 5 on the substrate 2 positioned along the right side or along the upper/lower sides of the memory chip 1A are examples thereof. Such featured aspects are included also in new claim 38. Incidentally, the invention according to new claim 38 is inclusive of that set forth in independent claims 16 and 29.

New claims 30-33 further define the invention according to new claim 29. Namely, claims 30, 31, 32, 33, 34 and 35 are similar to claims 17, 24, 25, 26, 27 and 28, respectively, but are combined differently therefrom. New claims 36 and 37 further characterize the memory card, according to claims 16 and 29, as containing also a cap covering the main surface of the substrate (e.g., see resin cap 4 in Fig. 7, *et seq.*). The set forth "cap" is also featured in new independent claim 38. It is submitted, a memory card as that now set forth in claims 16-28, claims 29-37 and claim 38 is a clear and patentable improvement over that previously known.

According to the outstanding Office Action, claims 16-28 were rejected under 35 USC §102(a) as anticipated by or, alternatively, under 35 USC §103(a), as being obvious over Kanemoto et al. As will be shown hereinbelow, the invention according to claims 16-28, as now amended, and, moreover, according to newly presented claims 29-38, it is submitted, could not have been anticipated nor rendered obvious in the manner as that alleged in these rejections. Therefore, insofar as presently applicable, to the currently pending claims, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

To reiterate, the invention according to each of independent claims 16, 29 and 38 can be said to relate to a memory card such as one having a memory chip such as a flash memory chip (e.g., 1A in Figs. 7-8) mounted on a substrate (e.g., base substrate 2), another semiconductor chip (e.g., control chip 1B) stacked on the memory chip, "first electrodes" and "second electrodes" (e.g., 5) formed on the main surface of the substrate and "first wires" and "second wires" for effecting electrical connections between the bonding pads of the respective chips with the corresponding ones of the first and second electrodes. The memory card according to these claims also calls for resin sealing the first and second semiconductor chips, the first wires, the second wires and the plurality of first electrodes and plurality of

second electrodes. According to claim 36 (dependent on claim 29), claim 37 (dependent on claim 16) and in independent claim 38, moreover, the resin sealed components of the memory card are further covered by a "cap" (e.g., 4 in Fig. 7), although not limited thereto. According to independent claims 16 and 38, the sets of first and second wires are disposed such that they are crossing over respectively different sides of the first semiconductor chip, in a plan view thereof and with regard to independent claims 29 and 38, the "first electrodes" and "second electrodes", which are formed on the main surface of the substrate, are respectively positioned along different sides of the first semiconductor chip, which is mounted on the substrate. Such a schemed construction as that now called for in claims 16+, 29+ and 38 was neither disclosed nor suggested from Kanemoto et al's disclosure.

Kanemoto et al disclosed a resin sealed semiconductor device which includes a stacking arrangement of a first semiconductor chip and a second semiconductor chip, the resin sealed semiconductor device being electrically connected to the wiring board via a plurality of leads which are bent and molded into one of surface mount lead configurations, for example, a "gull wing type lead configuration." However, Kanemoto et al's scheme neither disclosed nor suggested a schemed construction as that now set forth in claims 16+, 29+ and 38. In this regard, Figs. 49-51 in Kanemoto et al, which were applied with regard to the presently outstanding rejections, will be discussed.

The resin sealed semiconductor device 100 does contain a stacked bonded arrangement of a lower semiconductor chip 112 having a memory circuit such as an EEPROM (or flash memory) and an upper semiconductor chip 110 which has a control circuit for controlling the memory chip 112. However, as can be seen from Fig. 51 in Kanemoto et al, both the lower flash memory chip 110 as well as the upper control circuit semiconductor chip 112 of the resin encapsulated device 100

feature an electrical connection scheme with the wiring board (e.g., 161 in Fig. 49) which requires the crossing over of wires of both of the chips at each of the sides (i.e., peripheral edges) of the lower memory chip 112, in clear contradistinction with that according to the present invention. Accordingly, even though the effective size of the CF card (compact flash card) according to Kanemoto et al is made smaller as a result of implementing a stacking arrangement of the memory and control chips (see column 29, lines 20-26), the size reduction thereof, at least insofar as the thickness of the realized memory card, is limited with regard to Kanemoto et al's scheme since the loop height especially of the upper control chip wires in Kanemoto et al's scheme must be sufficiently high so as to avoid contact with the bonding wires of the lower memory chip that are crossing over the same side (i.e., the same peripheral edge) of the lower memory chip. According to the present invention, however, such undesired contact cannot result since the bonding wires (or first wires) associated with the first semiconductor chip are crossing over a different side (peripheral edge) of the first semiconductor chip than the bonding wires (or second wires) associated with the second semiconductor chip.

According to independent claim 16 and, likewise, in new claim 38, the "first wires" which electrically connect each of the bonding pads of the first semiconductor chip (e.g., memory chip or flash chip 1A) with a corresponding first electrode (formed on the substrate) are crossing over one side of the first semiconductor chip, in the plan view thereof, and the "second wires" (e.g., 6, in Figs. 7-8) which electrically connect the second semiconductor chip (e.g., control chip 1B) with a corresponding second electrode (e.g., 5 formed on the substrate 2) are crossing over another side of the first semiconductor chip, in a plan view thereof, different from the side over which the first wires are crossing. Such a schemed construction

as that called for in independent claim 16 and 38 was neither disclosed nor would have been realizable from Kanemoto et al's disclosure.

According to independent claim 29 as well as newly presented independent claim 38, in addition to the setting forth of first wires electrically connecting each of the bonding pads of the first semiconductor chip with a corresponding one of the plurality of first electrodes (formed on the substrate), and second wires for electrically connecting each of the bonding pads of the second semiconductor chip with a corresponding one of the plurality of second electrodes, the memory card further calls for the first electrodes to be positioned along one side of the mounted first semiconductor chip (e.g., the arrayed electrodes 5 along the left side or left peripheral edge of the memory chip 1A) and the set forth second electrodes to be positioned along another side of the mounted first semiconductor chip (e.g., terminals 5 arrayed along the right hand side and/or upper/lower side of the memory chip 1). Such a schemed placement or arraying of the first electrodes and the second electrodes, respectively, avoids any possibility of undesired contact between that of a first wire and a second wire. Such a schemed construction, it is submitted, is clearly contrary to that taught by Kanemoto et al. Therefore, since the placement of the plurality of first electrodes and the plurality of second electrodes on the substrate would lead to a wiring scheme such that contact between the "first wires" and "second wires" would clearly be avoided, the size and thickness of the memory card can be addressed without the prospect of contact between a first bonding wire (associated with a memory chip) and a second bonding wire (associated with the control chip).

A further aspect of the invention such as set forth in dependent claims 36 and 37 as well as in independent claim 38 calls for a "cap" which covers the main surface of the substrate (e.g., 4 in Fig. 7). This is in addition to the first

semiconductor chip (e.g., flash memory chip), the second semiconductor chip (e.g., a control chip), the first wires, the second wires, the plurality of first electrodes and a plurality of second electrodes being resin sealed. It is submitted, a scheme such as that set forth in independent claims 16, 28 and 38 and also with regard to the corresponding dependent claims thereof could not have been anticipated nor rendered obvious from Kanemoto et al for at least the above reasons. The same arguments are also applicable with regard to the further limiting aspects for various ones of the corresponding dependent claims thereof.

Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration and withdrawal of the outstanding alternative art rejections as well as a favorable action on all of the presently pending claims, i.e., claims 16-38, and an early formal notification of allowability of the above-identified application is respectfully requested.

In reply to the Examiner's refusal to consider the listed foreign patent documents with regard to the earlier filed IDS, enclosed herewith is a newly prepared listing of the same three foreign patent documents in form PTO/SB/08a along with copies thereof for the Examiner's consideration. The submission of the copies of these documents is being provided as a courtesy to the Examiner. That is, the Submission of a new listing of the three earlier listed foreign patent documents does not constitute a newly filed IDS since the earlier submitted IDS, it is believed, was in compliance with the appropriate rules and USPTO guidelines directed thereto.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, she is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at

the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. If any costs are due in connection with the filing of this paper, please charge them to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.39155VC2), and please credit any excess fees to such deposit account.

Respectfully submitted,
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